Analysis of Temperature Distribution on Power Switches Arrangements in Power Converter for Switched Reluctance Motor Drive

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***Abstract*—This paper presents a temperature rise simulation model of power converter for switched reluctance motor (SRM) drive. The accuracy of the model is verified by comparing experimental results with simulation data. Furthermore, three types of power switches arrangements and two PWM chopping schemes are studied with the present model for reduction of the maximum temperature rise. It is shown that the PWM chopping alternately scheme, the upper row power switches and lower row power switches installed on the two sides of midline of the heat sink contributes to the decrease of the maximum temperature rise of the power converter.**

Index Terms—**Thermal conductivity, temperature, motors.**

. INTRODUCTION

Switched reluctance motor (SRM) drive has the good prospect for applications on coal mines aircrafts and some industrial domain [1]-[5] because of the robust features. The electromagnetic loss causes the temperature rise in SRM, and the power losses of power transistors and freewheeling diode including switching losses and on-state losses causes the temperature rise in power converter. The power converter is the weakest part of the drive system. The temperature rise in power converter should be limited in order to avoid thermal breakdown of power transistors and freewheeling diodes because of over-heating of power converter. Therefore, it is very important and indispensable to set up an accurate thermal model of power converter of SRM, describe the distribution of temperature rise on power converter and obtain the well power switches arrangement scheme.

I. STRUCTURE OF POWER CONVERTER

The main circuit topology of the developed power converter in switched reluctance motor drive for large current mode of electric vehicles is a three-phase asymmetrical half-bridge circuit, which shown in Fig. 1. There are six power transistors and six freewheeling diodes in the main circuit, there are two power transistors and two freewheeling diodes in each phase.

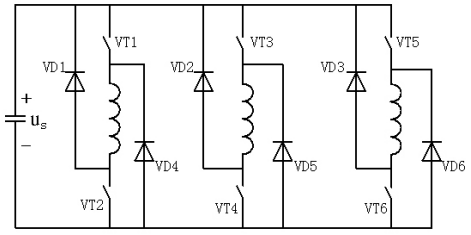


Fig. 1. Main circuit topology of the power converter.

There are 12 temperature rise test points with one test point on each power MOSFET shown in Fig. 2, which are chosen to measure the surface temperature rise of 12 power MOSFETs. The ambient temperature is 14.5 ^{0}C.

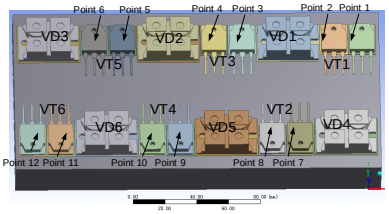


Fig. 2. Practical structure of power converter main circuit and 12 test points.

II. TEMPERATURE RISE SIMULATION MODEL

The mathematical formulation of the heat transfer of heat sink for the temperature rise simulation model of the power converter is as follows based on Cartesian coordinate system.

$$\phi_{in} = \phi_{out} \tag{1}$$

$$\sum_{i=1}^{m} P_i = h(T - T_a)S + \varepsilon\sigma(T^4 - T_a^4)S \tag{2}$$

$$\rho c \frac{\partial T}{\partial \tau} = \frac{\partial}{\partial x}(\lambda \frac{\partial T}{\partial x}) + \frac{\partial}{\partial y}(\lambda \frac{\partial T}{\partial y}) + \frac{\partial}{\partial z}(\lambda \frac{\partial T}{\partial z}) + \varphi \tag{3}$$

where, ϕ_{in} is the heating power generated by the power converter (units: W or J/s), ϕ_{out} is the radiating power from the heat sink surface to ambient (units: W or J/s), P_i is the heat power of ith power switches (units: W), m is the number of power switches, h is the convection heat transfer coefficient [units: W/(m^2·^{o}C)], T is the heat sink temperature (units: ^{o}C), T_a is the ambient temperature (units: ^{o}C), S is the surface area of heat sink (units: m^2), ε is the thermal radiation coefficient (no units), σ is the Boltzmann constant 5.67×10^{-8}W/(m^2·^{o}C^4), ρ is the material density (units: kg/m^3), c is the specific heat capacity [units: J/(kg·^{o}C)], τ is the time (units: s), λ is the thermal conductivity [units: W/(m·^{o}C)], φ is the heating energy by per unit time and per unit volume [units: J/(m^3·s)].

Boundary conditions:

1) The interfaces between the power switches and the gasket, the interfaces between the gasket and the heat sink meet as follows, a) the contact parts between material I and II has the same temperature,

$$T_I = T_{II} \tag{4}$$

where, T_I is the temperature of material I (units: ^{o}C) and T_{II} is the temperature of material II (units: ^{o}C). b) the density of heat flow rate is equal along the normal vector n of the contact

parts between material I and II,

$$(\lambda\frac{\partial T}{\partial n})_I = (\lambda\frac{\partial T}{\partial n})_{II} \quad (5)$$

2) Other surfaces in objects meet:

$$-\lambda(\frac{\partial T}{\partial x}+\frac{\partial T}{\partial y}+\frac{\partial T}{\partial z}) = h(T_a - T_f) \quad (6)$$

where, T_f is the temperature of other surfaces (units: ^oC).

3) The initial temperature of the object is the ambient temperature.

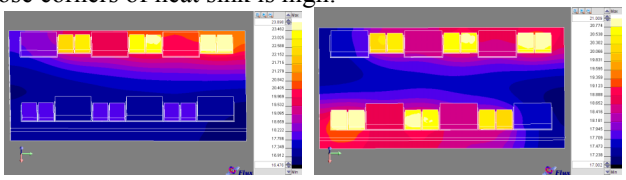
The temperature rise of power switches, ΔT, can be expressed as:

$$\Delta T = T_j - T_a = PR_{ja} \quad (7)$$

where, T_j is the junction temperature of power switches (units: ^oC), R_{ja} is the thermal resistance from junction to ambient (units: $^oC/W$).

III. Optimization of Power Switches Arrangement

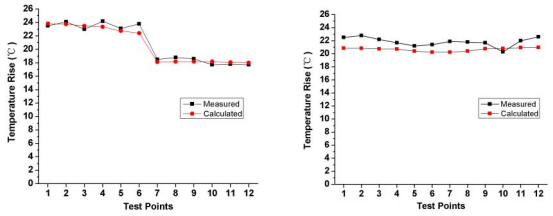
1) Upper Chopping: Fig. 3a) shows that the simulated steady state temperature rise distribution of the upper row power switches is much higher than that of the lower row ones and the temperature rise of power switch decreases from right to left. The maximum temperature rise, 23.9^{o}C, is in VT1 which is at the upper corner of the heat sink. Because the heating power of upper main switches is larger than that of upper freewheeling diodes and the thermal resistance of heat sink at the corner of heat sink is very high. 2) Chopping Alternately: The simulated steady state temperature rise distribution of arrangement I with chopping the upper and lower power MOSFETs alternately is shown in Fig. 3b). The maximum temperature rise, 21.0^{o}C, is in VT1 and VT6 which are at the upper corner of the heat sink and at the lower corner of the heat sink since the thermal resistance of heat sink at those corners of heat sink is high.



a) upper chopping b) chopping alternately

Fig. 3. Temperature rise distribution of arrangement I.

The comparison of experimental results and simulated results in steady state temperature rise at 12 test points is given in Fig. 4 a) upper chopping and b) chopping alternately, respectively. It is shown that the simulated data agree well with the experimental results with the same trend and variational magnitude. The error range is a) from -5.8% to 2.7%, b) from -8.6% to 2.6%.

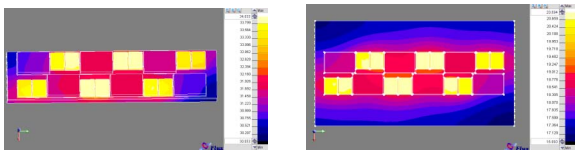


a) upper chopping b) chopping alternately

Fig. 4. Comparison of experimental results and simulated results.

The maximum temperature rise at the 12 points with chopping alternately is lower than that with upper chopping in experiments and simulation since the average heating power is distributed on the upper row power switches and the lower row power switches uniformity.

In order to save the heat sink board, reduce the volume and weight of the heat sink, a half width heat sink is adopted while the other geometric parameters and physical properties remain the same. The simulated steady state temperature rise distribution with chopping alternately is shown in Fig. 5a). The maximum temperature rise, 34.0^{o}C, is in VT3 and VT4 since the thermal coupling between upper rows and lower rows is strong, and the thermal resistance of heat sink with half width is higher than that with the original width. The simulated steady state temperature rise distribution with chopping alternately is shown in Fig. 5b), while the upper row power switches and lower row power switches are installed on the two sides of midline of the original width heat sink. The maximum temperature rise, 20.9^{o}C, is in VT3 and VT4, which is the lowest maximum temperature rise since the thermal resistance of heat sink is small.



a) half width b) original width

Fig. 5. Temperature rise distribution of arrangement III.

IV. Conclusion

In this paper, a temperature rise simulation model of power converter for switched reluctance motor drive has been introduced under constant convective heat transfer. This model can optimize the power switches arrangements, predict the temperature rise distribution of power converter, and optimize PWM chopping scheme. The accuracy of the model is verified by comparing experimental results with simulation data. The error is mainly caused by that the current in two parallel power MOSFETs as a main switch unit are not equal, and contact thermal resistance between every two materials is neglected.

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