Reduction of EMI Effects in Motor Drives and Complex Power Electronic Systems

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Abstract —This paper presents a systematic way to design optimal filters for line drivers and analog signal paths through modeling and simulation. The goal is to mitigate the effects of Electro-Magnetic Interference (EMI), particularly in an environment with high switching speed enabled by high band-width Silicon Carbide (SiC) and Gallium Nitride (GaN) semiconductor technologies. Frequency based analysis of EMI coupling between power and signal tracks, design of optimal low pass filters with maximum noise reduction and minimum signal delay, and efficient transient analysis to verify proper filter components are among the methods provided to optimally reduce the impact of EMI in motor drive and other power electronic applications.

I. Introduction

High band-width Field Effect Transistor (FET) technologies such as GaN and SiC have the ability to drastically reduce switching losses in motor drives and other power electronic applications [1]. This can lead to higher switching frequencies, thus reducing the size of energy storage components such as inductors and capacitors. However, these types of switches introduce new technical challenges. The fast switching currents and voltages induce transient voltages on the data busses and analog signals. For instance, the induced voltage on the wires carrying gate signals to the gate drivers can lead to unintentional firing of the semiconductor switches. Typical line drivers are made from logic gates that are considered in a low input state if the input voltage is below 1V, depending on the particular driver. Therefore, an induced voltage higher than 1V can be considered as a gate command. Numerous studies have been conducted to improve modeling of EMI [2] or to reduce the EMI emissions [3]-[5]. However, no particular method has been introduced to deal with EMI induced voltage on a digital signal and current engineering methods are mostly based on "rule of thumb".

The objective of this work is to study the effects of EMI in applications with high switching frequencies. Moreover, optimal passive filtering is introduced to reduce the effects of EMI. The "rule of thumb" for preventing a logic gate from getting a false "high" signal is to load the input of the logic gate using a 1kΩ to 20kΩ resistor. However, it is not known if this is sufficient. Additionally, to prevent current and voltage sensors from suffering from EMI effects, the analog signals must be converted to digital signals before the traces become large enough to pick up significant amounts of EMI. This would typically result in additional Analog to Digital Converters (ADCs) located close to the sensors. However, this method results in added cost and complexity to the converter. Another solution is to use low pass filters with the cut off frequency set at the lowest possible value to ensure controllability. However, low pass filters will add phase shift to the signal. Hence, the stability of the controller will be reduced. This leads the engineer to design the optimal filter to maximize the reduction in EMI while minimizing the phase shift.

II. Determining EMI Frequencies of Interest

The first step to develop a proper EMI filter is to determine the optimum cut off frequency. In large systems, finite element modeling of the system is required to estimate the optimum cut off frequency. Figure 1 illustrates a 12kW water cooled converter designed for motor drive applications.

HFSS is used for finite element modeling of this converter. The model is shown in Figure 2. Some simplifications have been made while modeling and only one of the gate drivers is modeled.

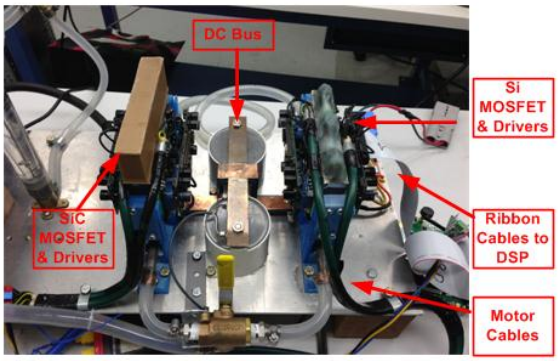

Fig. 1. 12kW water cooled motor drive featuring SiC and Si MOSFETs

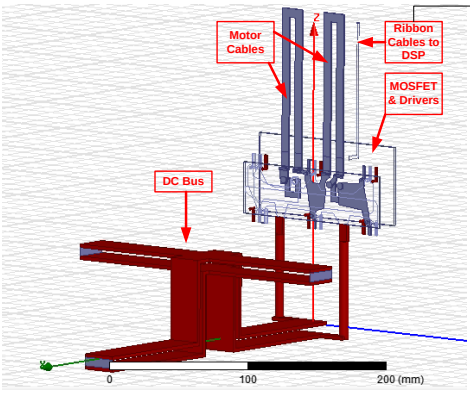

Fig. 2. HFSS model of 12kW water cooled motor drive.

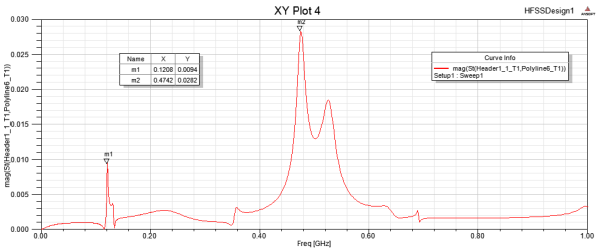

Fig. 3. S-Parameters between motor terminals and logic gate.

One method to determine the best filter is to introduce RLC filters. Iterative transient simulations are performed. After each step, RLC values are changed until the effects of EMI are minimized on the signal of interest. This solution method would be very time consuming. For this particular solution (given the large 3d geometry) a 50 ns transient solution requires more than one day to solve. Therefore it is desirable to generate one set of frequency based solutions and determine the S-parameters between the switching nodes and the data cables (i.e. ribbon cables in Figure 2). These S-parameters can be exported to other software to calculate the transient response without further field solutions. Figure 3 shows the S-parameter between the motor terminals and the logic gate. It can be observed from Figure 3 that the majority of the transferred energy is transmitted at 474 MHz (and higher) and 121 MHz.

III. Design of Optimal Filter And Simulation Method

Ansoft Designer is employed to simulate the HFSS model during a 30A current ramp with a 13 ns rise time. 13 ns rise time is chosen based on the switching times of the SiC components. Typical RC and RLC low pass filters were designed at various cutoff frequencies corresponding to the peaks in the Figure 3. These cut off frequencies and filter components are listed in Table I. Moreover, the parasitic resistance and capacitance of a typical logic gate is included in each model.

TABLE I
FILTER CUT OFF FREQUENCY, COMPONENTS, AND RISE TIMES

fc (MHz)	RC Filter		Rise Time* (ns)	RLC Filter			Rise Time* (ns)
	R (Ω)	C (pF)		R (Ω)	L (μH)	C (pF)	
600	75	10	0.6	160	0.022	3.5	0.8
400	110	3.5	0.9	51	0.01	15	1.2
110	150	10	1.8	200	0.15	15	4.0

*Rise time refers to the time to rise to 3.5V, the turn on voltage of a typical logic gate, given a 5V step input.

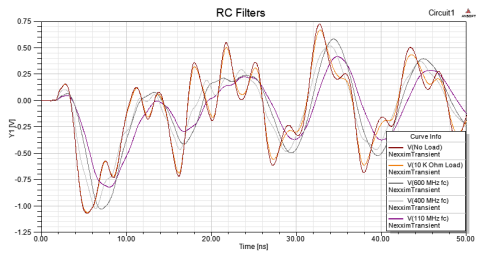

Fig. 4. Transient voltage waveforms on the logic gate under no load conditions, loaded with a 10kΩ resistor, and with RC low pass filters at cutoff frequencies of 600, 400, and 110 MHz, respectively.

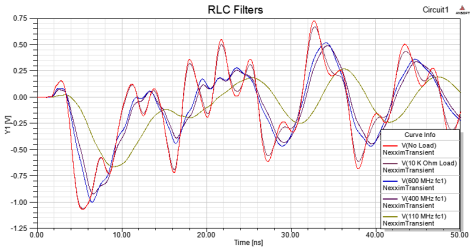

Fig. 5. Transient voltage waveforms on the logic gate under no load conditions, loaded with a 10kΩ resistor, and with RLC low pass filters at cutoff frequencies of 600, 400, and 110 MHz, respectively.

IV. Simulation Results

Figure 4 and Figure 5 show the simulated waveforms for RC and RLC filters, respectively. It can be observed that these filters can be effectively designed to reduce the impact of EMI generated due to low switching times. In the converter shown in Figure 1, the logic gates are in "high" state if the input voltage is greater than 1V. It can be observed that with no filters, the gate driver will read the "high" signal due to the induced voltage of 1.1V at 6ns. However, the designed RC filters can reduce the induced voltage by 25% while only delaying the signal by 1.8 ns. The RLC filter can reduce the induced voltage by 50% while delaying the on/off signal by 4.0 ns. Both filters will prevent false firing of the gate driver according to the model.

V. Conclusion

A detailed study to design filter components for data cables in a power electronic converter was presented. It was shown that finite element model of a power electronic converter can be used to design optimum filters for digital signals. These filters can designed effectively and efficiently to reduce the electro-magnetic interference caused by fast switching voltages and current on the logic signals while minimizing the signal delay.

VI. References

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